WHAT IS CLAIMED IS:

1. In a semiconductor wafer fabrication system that includes at least a track system and a scanner system, a method of compensating the fabrication system for deviations from nominal scanner system clock periodicity, the method comprising the following steps:

(a) operating said scanner system responsive to a signal from a scanner system clock;

(b) operating said track system responsive to a signal from a track system clock;

(c) pre-determining and inserting wait states as needed to avoid conflict for resources in said semiconductor wafer fabrication system; and

(d) determining deviation from nominal timing in said scanner clock and dynamically inserting time delay as needed in said semiconductor wafer fabrication system to compensate for such deviation.

2. The method of claim 1, wherein said scanner clock operates with a repetition rate equivalent to at least 90 wafers per hour throughput for said semiconductor wafer fabrication system.

3. The method of claim 1, wherein said scanner clock operates with a repetition rate equivalent to at least 160 wafers per hour throughput for said semiconductor wafer fabrication system.

4. The method of claim 1, wherein location and length of each said time wait at step (c) is determined by a computer system controlling, at least in part, said semiconductor wafer fabrication system.

5. The method of claim 1, wherein said semiconductor wafer fabrication system includes at least two robotic stations.

6. The method of claim 1, wherein said semiconductor wafer fabrication system includes at least three robotic stations.

7. The method of claim 1, wherein said semiconductor wafer fabrication system includes at least four robotic stations.

8. The method of claim 1, wherein step (c) and step (d) are carried out by a computer system.

9. The method of claim 1, wherein said track system operates responsive to a signal from said track system clock, and said scanner system operates responsive to a signal from said scanner system clock.

10. A semiconductor wafer fabrication system, comprising:

a scanner system operating responsive to a signal from a scanner system clock;

a track system operating responsive to a signal from a track system clock;

means for moving at least one wafer within said semiconductor wafer fabrication system;

means for inserting pre-planned wait states in said single-clock semiconductor wafer fabrication system to reduce conflict for resources in said semiconductor wafer fabrication system; and

means for dynamically inserting time delay as needed in said semiconductor wafer fabrication system to compensate for disturbance in periodicity of said scanner clock.

11. The semiconductor wafer fabrication system of claim 10, wherein said scanner clock operates with a repetition rate equivalent to at least 90 wafers per hour throughput for said semiconductor wafer fabrication system.

12. The semiconductor wafer fabrication system of claim 10, wherein said scanner clock operates with a repetition rate equivalent to at least 160 wafers per hour throughput for said semiconductor wafer fabrication system.

13. The semiconductor wafer fabrication system of claim 10, further including a computer system that controls, at least in part, said semiconductor wafer fabrication system.

14. The semiconductor wafer fabrication system of claim 10, wherein said means for dynamically inserting time delay includes a computer system.

15. The semiconductor wafer fabrication system of claim 14, wherein said computer system generates at least said scanner system clock.

16. The semiconductor wafer fabrication system of claim 10, wherein said means for moving includes at least two robotic stations.

17. The semiconductor wafer fabrication system of claim 10, wherein said means for moving includes at least three robotic stations.

18. For use in operating a semiconductor wafer fabrication system that includes at least a scanner system operating responsive to a signal from a scanner system clock, and a track system operating responsive to a signal from a track system clock, a computer readable medium storing a computer program that when executed carries out at least one of the following steps:

(a) determines deviations from nominal periodicity in said scanner system clock; and

(b) calculates and dynamically inserts time delay as needed in said semiconductor wafer fabrication system to compensate for said deviations.

19. The computer readable medium of claim 18, wherein said program when executed statically determines pre-planned wait states to minimize resource conflict within said semiconductor wafer production system.

20. The computer readable medium of claim 18, wherein said program when executed dynamically determines deviations from nominal periodicity in said scanner system clock, and calculates time delay needed to compensate for said deviations.